Paper No. 37

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MASAMICHI AZUMA, EIJI FUJII, YASUHIRO UEMOTO, SHINICHIRO HAYASHI, TORU NASU, YOSHIHIRO SHIMADA, AKIHIRO MATSUDA, TATSUO OTSUKI, MICHAEL C. SCOTT, JOSEPH D. CUCHIARO and CARLOS A. PAZ DE ARAUJO

Appeal No. 1998-1578
Application No. 08/543,827

HEARD[1]: March 6, 2001

Before JOHN D. SMITH, LIEBERMAN, and DELMENDO, Administrative Patent Judges.

DELMENDO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1 through 18 and

[1] Mr. Carl A. Forest argued for the appellants before this panel in a telephonic hearing conducted on the date noted.

28, which are all the claims pending in the subject application.

Claims 1 and 14 are illustrative of the claims on appeal and are reproduced below:

> 1. A method of making an integrated circuit capacitor, said method comprising the steps of:
> forming a metal nitride barrier layer having a thickness;
> annealing said metal nitride barrier layer in a barrier anneal step having a maximum temperature derived as a function of said thickness, said function including any value within a range one-hundred degrees greater than a line defined by the points (700EC, 1000 D) and (800EC, 3000 D), said maximum temperature being at least 675EC;
> then, after said above steps, forming a first electrode; thereafter
> forming a dielectric layer on said first electrode; and thereafter
> forming a second electrode on said dielectric layer.
>
> 14. A method of making an integrated circuit capacitor, said method comprising the steps of:
> forming a layer of titanium;
> forming a layer of titanium nitride on said layer of titanium;
> annealing said titanium and titanium nitride layers in a barrier anneal step having a maximum temperature derived as a function of said thickness, said function including any value within a range one-hundred degrees greater than a line defined by the points (700EC, 1000 D) and (800EC, 3000 D), said maximum temperature being at least 675EC;
> then, after said above steps, forming a first electrode; thereafter

forming a dielectric layer on said first electrode; and thereafter
forming a second electrode on said dielectric layer.

The subject matter on appeal relates to a method of making an integrated circuit capacitor. In the claimed method, a metal nitride barrier layer (e.g., a titanium nitride layer, claim 14) is deposited. Then the metal nitride layer is annealed in a barrier anneal step having a maximum temperature derived as a particular function of the thickness of the deposited metal nitride layer. Specifically, the maximum anneal temperature function includes any value within a range one hundred degrees greater than a line defined by the points (700EC, 1000 D) and (800EC, 3000 D), provided that the maximum anneal temperature is at least 675EC. After annealing, a first electrode, a dielectric layer on the first electrode, and a second electrode on the dielectric layer are formed. According to the appellants, anneal conditions outside the claimed maximum temperature range produce poor morphology in the form of surface irregularities, such as hillocks and porosity, which can cause shorting or degrade

performance in dielectric capacitor devices. (Appeal brief, page 4.)

As evidence of unpatentability, the examiner relies upon the following prior art references:

Larson	5,005,102	Apr. 2, 1991
Ho et al. (Ho)	5,175,126	Dec. 29, 1992

Also, we cite the following new prior art reference in a new ground of rejection:

Scott et al. (Scott)	5,514,822	May 7, 1996 (filed Oct. 6, 1993)

Appealed claims 1 through 18 and 28 stand rejected under 35 U.S.C. § 103 as unpatentable over Larson in view of Ho.

Upon consideration of the entire record, we agree with the appellants that the aforementioned rejection is not well founded. Accordingly, we reverse the examiner's rejection. However, pursuant to 37 CFR § 1.196(b) (1997), we enter two new grounds of rejection.

In considering the examiner's rejection, we need to address only claims 1 and 14, the independent claims. In re

Fine, 837 F.2d 1071, 1076, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988).

Under 35 U.S.C. § 103, the initial burden of establishing a prima facie case of obviousness rests on the examiner. In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). In this case, it is our determination that the examiner has not met the initial burden of proof.

Larson describes a method for forming a multilayer capacitor structure in an integrated circuit. (Column 1, lines 33-35.) In particular, Larson teaches an embodiment in which the structure comprises a bottom electrode **114** having three layers (titanium layer **120**, titanium nitride layer **124**, and platinum layer **126**) over a substrate **112**, a dielectric layer **116**, and a top electrode **118** comprising three additional layers (platinum layer **130**, titanium layer **132**, and aluminum layer **134**). (Figure 2; column 3, line 34 to column 4, line 28.) According to Larson, the titanium nitride layer **124** has a thickness of approximately 0.1 micron (1000 D) and serves, inter alia, as a diffusion barrier layer. (Column 3, lines 46-52.) Further, Larson states that

the platinum layers **126** and **130** can function as electrode plates.[2] (Column 3, lines 54-55; column 4, lines 9-10.)

Regarding the steps for making the structure, Larson teaches that the structure is constructed in an evacuation chamber, preferably in two separate evacuations or "pump downs," wherein the bottom electrode and the dielectric layer are constructed during the first pump down and the top electrode is constructed during the second pump down. (Column 3, lines 26-32.) Also, Larson states that various "known techniques," including but not limited to sputtering, can be used for depositing each of the layers. (Column 4, lines 28-36.)

The examiner admits that Larson "fails to teach annealing the titanium/titanium nitride layers, i.e. barrier layers, before depositing the dielectric and second electrode[s]." (Examiner's answer, page 4.) In addition, we note that Larson lacks any teaching as to the maximum anneal temperature-

[2] The appellants' specification states that platinum is one of the preferred materials for the electrodes. (P. 6, ll. 23-25.)

barrier layer thickness function as recited in appealed claims 1 and 14.

To account for this difference, the examiner relies on Ho. However, we share the appellants' view that the relied upon portion of Ho's teaching does not provide any teaching, motivation or suggestion for one of ordinary skill in the art to modify the method described in Larson so as to arrive at the appellants' claimed method.

Specifically, Ho describes a prior art process involving the use of rapid thermal annealers (RTAs) for improving the integrity of a barrier layer of titanium nitride sputtered onto a substrate, wherein the substrate is processed in a RTA at about 800EC to 900EC in nitrogen for 30 to 60 seconds. (Column 3, lines 13-19.) However, Ho also teaches that this prior art method is not "production worthy" and suffers from many problems including "numerous equipment failures" and "greater potential for warping substrates ." (Column 3, lines 26-49.) According to Ho, RTAs are primarily used in limited production modes, such as research and development. (Column 3, lines 49-51.)

However, as pointed out by the appellants (appeal brief, page 9), Ho is silent on the relationship between the maximum annealing temperature for the prior art RTA method and the thickness of the titanium nitride layer that is sputtered onto the substrate. Although the appellants have not really disputed the examiner's contention that "it is well known in the art that

the annealing temperature of any coating is a function of many 'cause effective variables' including thickness" (appeal brief, page 11; examiner's answer, page 7), the examiner has not presented any evidence to establish that the prior art RTA method discussed in Ho would be applicable for all barrier layer thicknesses (e.g., a titanium nitride barrier layer thickness of 0.1 micron (1000 D) as described in Larson) or for all structures (e.g., a capacitor as described in Larson).

Moreover, we agree with the appellants that the prior art references, as applied by the examiner, teach away from the appellants' claimed invention. A prior art reference teaches away if one of ordinary skill in the art, upon reading the reference, would have been (i) discouraged from following the path set out in the reference or (ii) led in a direction

divergent from the path that was taken by the applicants. In re Gurley, 27 F.3d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994).

Here, we observe that Ho describes many problems with prior art annealing methods that involve RTAs, even going as far to say that prior art RTAs "are not production worthy." (Column 3, lines 26-27.) Based on this disclosure, it is our opinion that one of ordinary skill in the art would have been discouraged from using the prior art RTA methods described by Ho. Accordingly, we see no reason why one of ordinary skill in the art would have combined Ho's teaching regarding prior art RTAs with the teaching of Larson to arrive at the appellants' claimed method.

For these reasons, we reverse the examiner's rejection of claims 1 through 18 and 28 under 35 U.S.C. § 103 as unpatentable over Larson in view of Ho.

New Grounds of Rejection

We enter the following new grounds of rejection pursuant to 37 CFR § 1.196(b).[3]

[3] Although our discussion is limited to appealed claims 1 and 14, the examiner and the appellants should consider the

Appealed claims 1 and 14, which are representative of all the appealed claims, are rejected under 35 U.S.C. § 103 as unpatentable over the combined teachings of Larson and Ho. Similarly, appealed claims 1 and 14 are rejected under 35 U.S.C. § 103 as unpatentable over the combined teachings of Scott and Ho.

We start by analyzing the scope of the appealed claims. Gechter v. Davidson, 116 F.3d 1454, 1460 n.3, 43 USPQ2d 1030, 1035 n.3 (Fed. Cir. 1997); In re Paulsen, 30 F.3d 1475, 1479, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994). It is axiomatic that in proceedings before the U.S. Patent and Trademark Office, claims

are interpreted by giving words their broadest reasonable meanings in their ordinary usage, taking into account the written description found in the specification. In re Morris, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); In re Zletz, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

---

new grounds of rejection on a claim-by-claim basis. If necessary, the examiner should enter additional new grounds of rejection on any or all the dependent claims.

Appealed claims 1 and 14 recite in part:

> annealing said metal nitride barrier layer in a barrier anneal step having a maximum temperature derived as a function of said thickness, said function including any value within a range one-hundred degrees greater than a line defined by the points (700EC, 1000 D) and (800EC, 3000 D), said maximum temperature being at least 675EC

Although appealed claims 1 and 14 recite a maximum annealing temperature as a function of the thickness of the barrier layer, these claims do not place any limitation on any minimum annealing temperature. Thus, giving the words of the above recitation their broadest reasonable interpretation, one of ordinary skill in the art would have understood appealed claims 1 and 14 to cover any annealing temperature below the recited maximum anneal temperature (e.g., 300 to 650EC).

This interpretation of appealed claims 1 and 14 is consistent with the written description found in the specification including the dependent claims. In particular, we observe that a preferred annealing temperature is described in the specification as including a temperature as low as 650EC,

which is well below the line defined by the points (700EC, 1000 D) and (800EC, 3000 D). (Page 7, lines 9-11; page 13,

lines 13-14; appealed claims 6 and 15) Thus, it is clear that the line defined by the points (700EC, 1000 D) and (800EC, 3000 D) is being used in appealed claims 1 and 14 to limit the maximum annealing temperature as a function of thickness, not to define any minimum annealing temperature.

It is true that the specification describes a "base barrier anneal temperature" that "varies from about 700EC for an effective barrier thickness of about 1000 D to about 800EC for an effective barrier thickness of about 3000 D." (Page 14, lines 12-17.) However, this feature is described as a preferred embodiment and is not recited in appealed claims 1 and 14. In this regard, a claim is not limited to a preferred embodiment described in the specification, especially where the language found in the claim is clear. Comark Communication, Inc. v. Harris Corp., 156 F.3d 1182, 1186-87, 48 USPQ2d 1001, 1005 (Fed. Cir. 1998); see also In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993).

We now turn to the teachings of the applied prior art references. To avoid repetition, we refer to our discussion above concerning the teachings of Larson.

With respect to Scott, we initially note that the application which matured into the Scott patent was filed on October 6, 1993, which is before the earliest effective filing date of the present application. Also, the Scott patent names Michael C. Scott, Carlos A. Paz de Araujo, and Larry D. MacMillan as joint inventors. By contrast, the present application does not include MacMillan as a joint inventor but instead lists nine additional inventors not named in the Scott patent. Thus, we determine that Scott is available as prior art under 35 U.S.C.
§ 102(e) (1999).

Scott teaches a method for making a capacitor comprising: (i) forming silicon dioxide **43** by thermal oxidation in a furnace; (ii) sputter depositing a titanium layer **44**, a titanium nitride layer **45**, and a platinum layer **46** to form a substrate **47**; (iii) using a BST precursor solution to form a dielectric BST layer **48** having a thickness of about 140 nm; (iv) annealing the BST in an oxygen furnace at 750EC; and then (v) depositing an electrode **49**. (Fig. 7; column 8, lines 21-46.)

Neither Larson nor Scott describes a step of annealing the titanium nitride barrier layer under the condition recited in appealed claim 1 or 14 before depositing the platinum layer. However, Ho teaches as follows:

> Titanium nitride (TiN) is used as a barrier layer. However, TiN as sputtered suffers from two defects. First, TiN has a columnar structure. If a transmission electron micrograph were taken of the TiN, the TiN would appear as groups of columns or grains. The gaps between the columns are referred to as grain boundaries. Grain boundaries cause problems with barrier layers. The grain boundaries form a path through which the metal can migrate to reach the underlying substrate. If the metal migrates through the barrier layer, spike formation or metal diffusion into the substrate can occur.
>
> Second, sputtering TiN itself causes a problem. A simple overview of sputtering techniques will indicate how the problem develops. A sputtering chamber is comprised of the following parts: a substrate, a target, the sputtering chamber itself, gases, and a power generator. The power generated can be direct current (DC), radio frequency (RF), etc. The generator ionizes the gas to form a plasma. The plasma is directed toward the target. In this case, reactive sputtering is utilized. The nitrogen in the plasma reacts with the surface of a titanium target to form a thin layer of TiN. In addition, the plasma hits the target causing the TiN to be stripped away from the target. The TiN coats the substrate and the walls of the sputtering chamber.
>
> Sputtering has problems. If the sputtering occurs faster than the plasma reaction at the target (converting the surface titanium to TiN), some titanium will be sputtered form [sic, from] the target before it si [sic, is] converted to TiN. The

> titanium is incorporated into the sputtered film. Also, the bombardment of the plasma onto the target can generate chemical reactions. The plasma can strip the nitrogen and titanium atoms from one another with a TiN molecule. Anytime sputtering is used to deposit the TiN barrier layer, both TiN and titanium will be incorporated into the sputtered film. Within the sputtered TiN film, there will be titanium-rich areas. Compared to TiN, titanium is more reactive with the substrate and etchants. The titanium is more likely to form unwanted compounds (such as titanium silicide, $TiAl_3$, TiAlSi, etc.) or to be etched away more readily than the TiN. [Underlining added; col. 1, l. 54 to col. 2, l. 29.]

Further, Ho teaches that when a metal is sputtered on top of TiN during the same evacuation cycle, the integrity of the barrier layer is "unacceptable," causing "spike formation or metal diffusion into the substrate." (Column 2, lines 30-41.)

To avoid these problems, Ho describes an "atmospheric furnace" process in which a sputtered TiN barrier layer is annealed prior to subsequent metal deposition. (Column 3, lines 52-68.) Specifically, this "atmospheric furnace" process applies to "any device where a TiN barrier will be used between a layer or layers of metal and underlying

semiconductor." (Column 5, lines 26-29.) According to Ho, this process involves annealing the TiN layer at a temperature range of 300EC to 650EC for greater than 80 minutes. (Column 6, lines 57-66.) It is important to note that Ho does not place any particular restriction on the thickness of the barrier layer. The appellants acknowledge as much. (Appeal brief, page 9.) Thus, it follows that Ho's improved process applies to any typical prior art TiN barrier layer.

From these facts, we determine that one of ordinary skill in the art would have found it prima facie obvious to modify the processes described in either Larson or Scott by annealing the TiN barrier layer at 300EC to 650EC for greater than 80 minutes using Ho's "atmospheric furnace" process, thus arriving at a
method encompassed by appealed claims 1 or 14, with the reasonable expectation of obtaining all of the advantages described in Ho including the prevention of spike formation or metal diffusion into the substrate. Any of the annealing temperatures described in Ho is encompassed by appealed claims 1 or 14.

The appellants argue that Ho teaches a fixed annealing temperature without regard to the thickness of the barrier layer. (Appeal brief, page 9.) We are not persuaded by this argument. While the claims on appeal recite a maximum annealing temperature as a function of barrier layer thickness, they do not recite a similar relationship for the minimum annealing temperature. Nor do the appealed claims recite any direct relationship between the actual annealing temperature and the barrier layer thickness. Moreover, the appellants do not really dispute the examiner's assertion that barrier layer thickness is a result-effective variable in annealing. (Appeal brief, page 11; examiner's answer, page 7.) We therefore determine that one of ordinary skill in the art would have selected an annealing temperature and an annealing time from Ho by taking into consideration the thickness of the barrier layer.

The appellants rely on the declaration of Dr. Araujo, filed July 20, 1995, as evidence of unexpected results. (Supplemental

reply brief, pages 10-12.) However, we are unclear as to how the evidence is even germane to appealed claims 1 and 14 as they relate to the applied prior art. As we have discussed above, appealed claims 1 and 14 read on any annealing temperature below the recited maximum anneal temperature (e.g., 300 to 650EC).

Even assuming that the evidence is germane to appealed claims 1 and 14, the showing of unexpected results must be commensurate in scope with the degree of patent protection sought. In re Dill, 604 F.2d 1356, 1361, 202 USPQ 805, 808 (CCPA 1979) ("The evidence presented to rebut a prima facie case of obviousness must be commensurate in scope with the claims to which it pertains."). Here, appealed claim 1 reads on any metal nitride barrier layer. Further, both appealed claims 1 and 14 read on a wide range of annealing temperatures, any first electrode, any dielectric layer, and any second electrode. It is not clear on this record how the evidence, which appears to be limited to a BST film formed on a Pt/TiN/Ti/D-PS/SiO_2/Si substrate at a limited number of

annealing temperatures, is even remotely commensurate in scope with the claims.

Also, the declarant refers to Figures 11 through 14, but the quality of the photomicrographs as found in the record are so poor that no reasonable conclusion is possible.

In summary, we have reversed the ground of rejection advanced on appeal by the examiner. However, we have entered new grounds of rejection of appealed claims 1 and 14 pursuant to 37 CFR § 1.196(b) (1997).

The decision of the examiner is reversed.

Time for taking action

This decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b) (1997). 37 CFR § 1.196(b) provides that "[a] new ground of rejection shall not be considered final for the purposes of judicial review."

37 CFR § 1.196(b) also provides that the appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (37 CFR § 1.197(c)) as to the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .
>
> (2) Request that the application be reheard under 37 CFR § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED
37 CFR § 1.196(b)

JOHN D. SMITH)
Administrative Patent Judge)
)
)
)

	)	BOARD OF PATENT
PAUL LIEBERMAN	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
	)	
ROMULO H. DELMENDO	)	
Administrative Patent Judge	)	

RHD/kis

CARL A. FOREST
DUFT GRAZIANO & FOREST PC
1790 30TH ST SUITE 140
BOULDER CO 80301-1018